Development of Trigger and Readout Electronics for the ATLAS New Small Wheel Detector Upgrade

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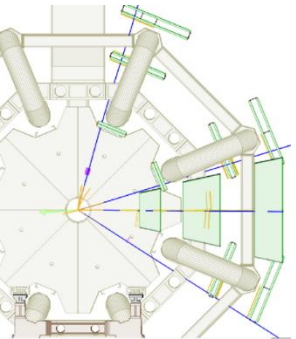


MEETING OF APS PARTICLES AND FIELDS

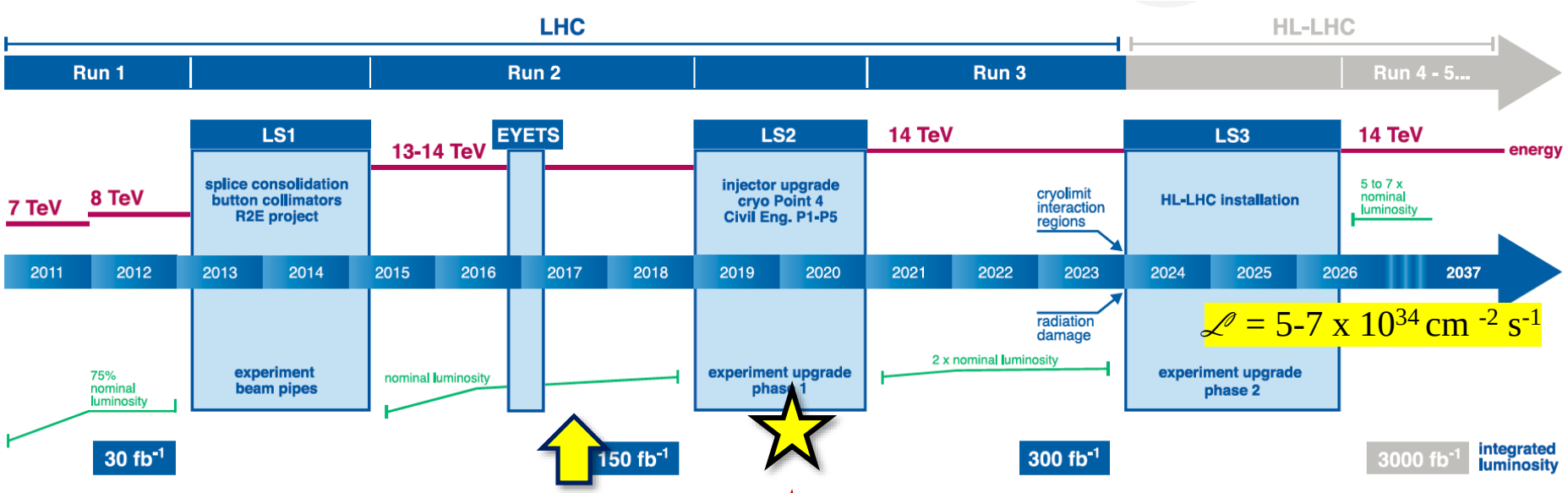
Fermilab , IL, USA

AUGUST, 03, 2017

Outline

- Introduction: ATLAS Muon New Small Wheel Upgrade
- New Small Wheel Trigger and Readout Electronics Chain
  - ASICs
  - On detector Front-end Boards
  - On detector Trigger Data Preparation Boards
  - Off detector Trigger Processor
- Radiation qualification for electronics and Integration Efforts
- Conclusions

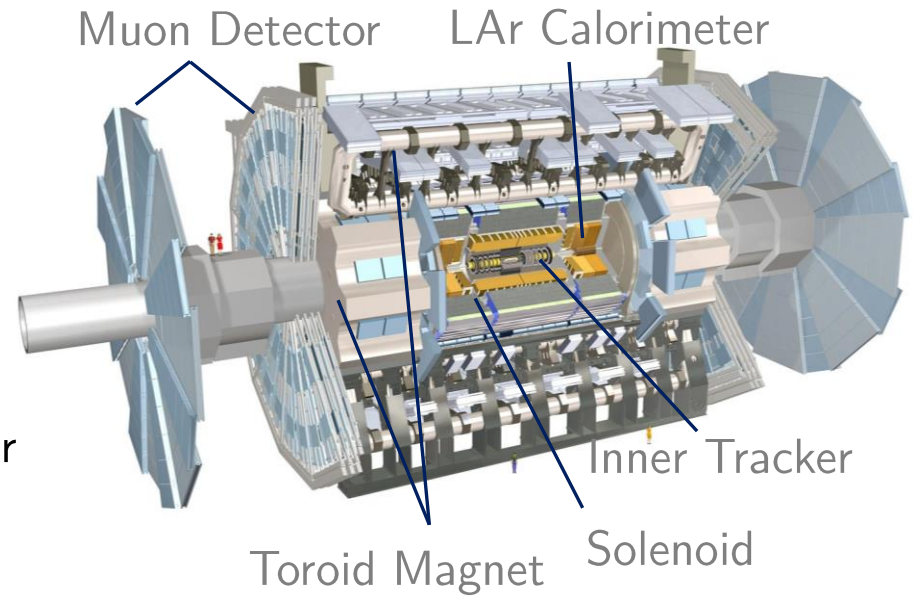
Introduction – LHC and ATLAS upgrade schedule



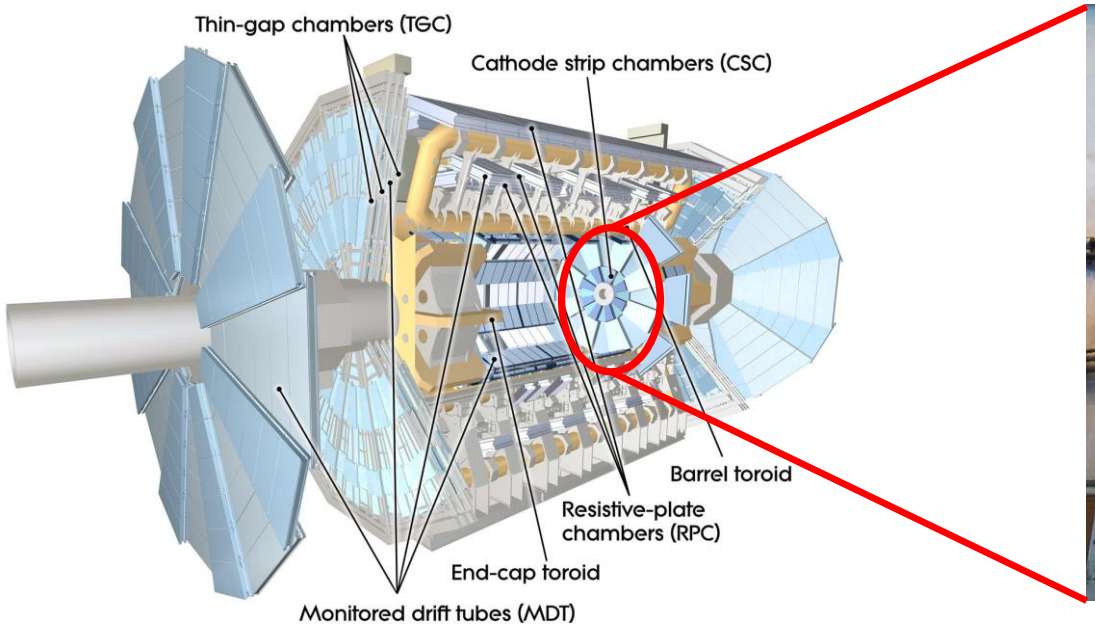
We Are Here!

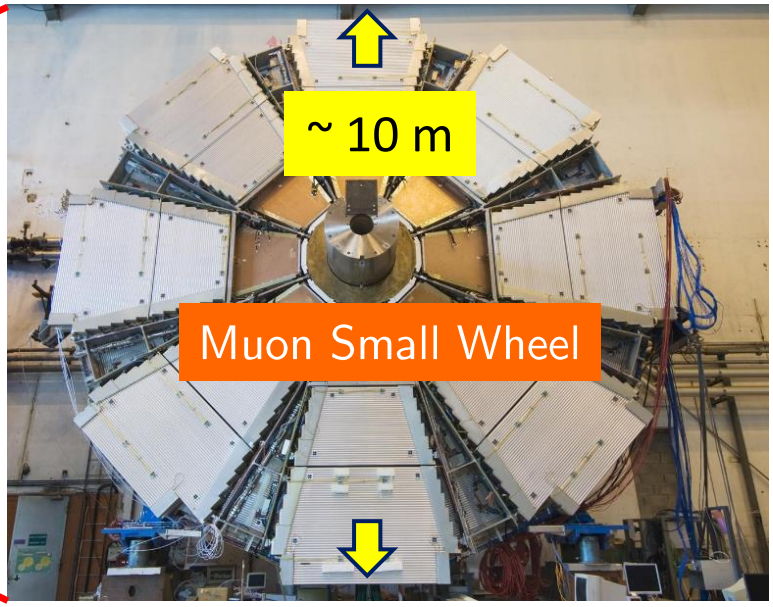
ATLAS Main Upgrades

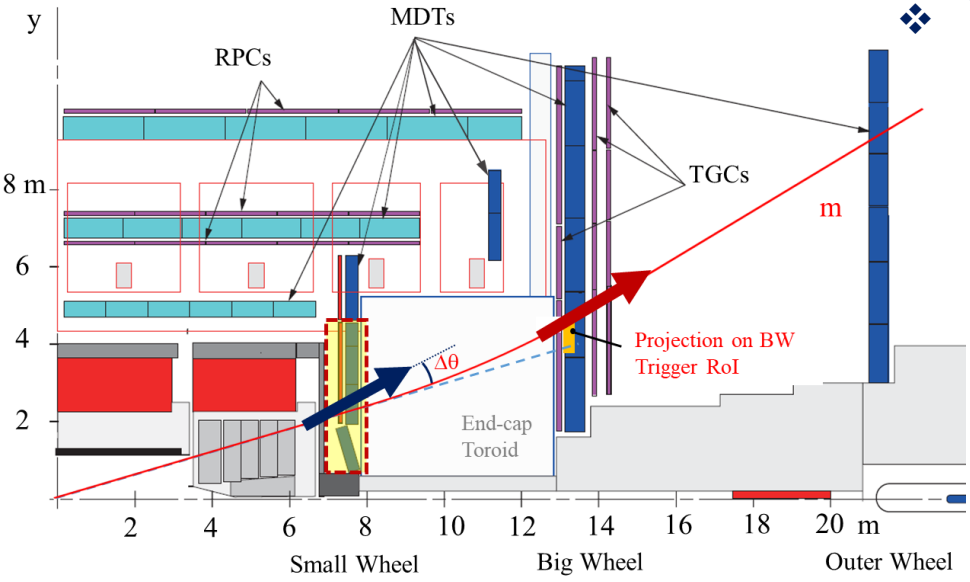
- Phase-0: Insertable B-Layer (IBL) in LS1
- Phase-1: Muon New Small Wheels (*Kawamoto, T., et al., New Small Wheel TDR, 2013*), Calorimeter trigger, Fast Tracker
- Phase-2: New Inner Tracker, New Trigger architecture, Muon Spectrometer ...



Introduction – ATLAS Muon New Small Wheel Upgrade



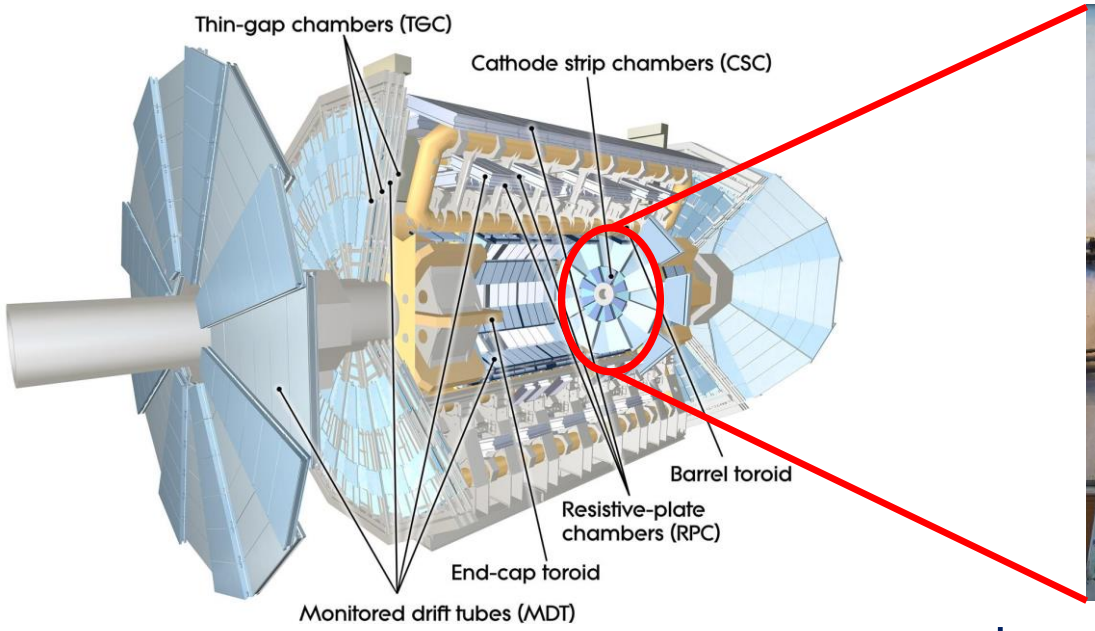


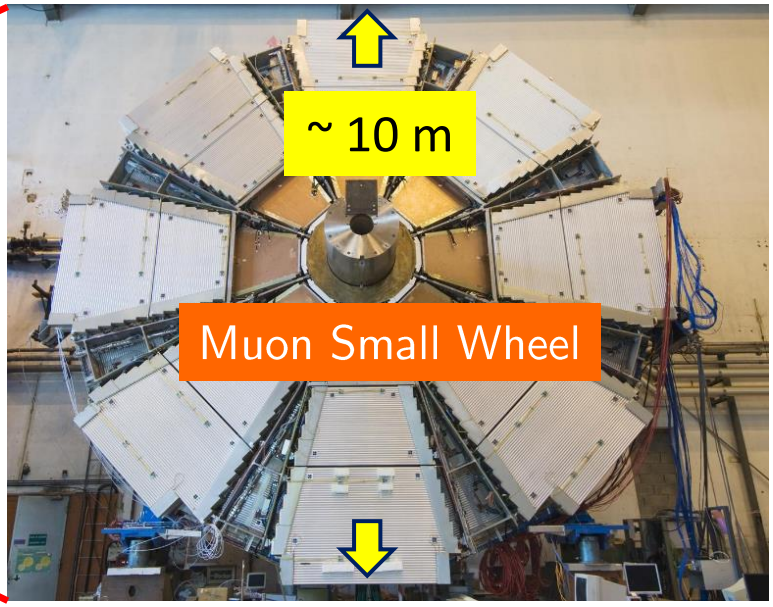


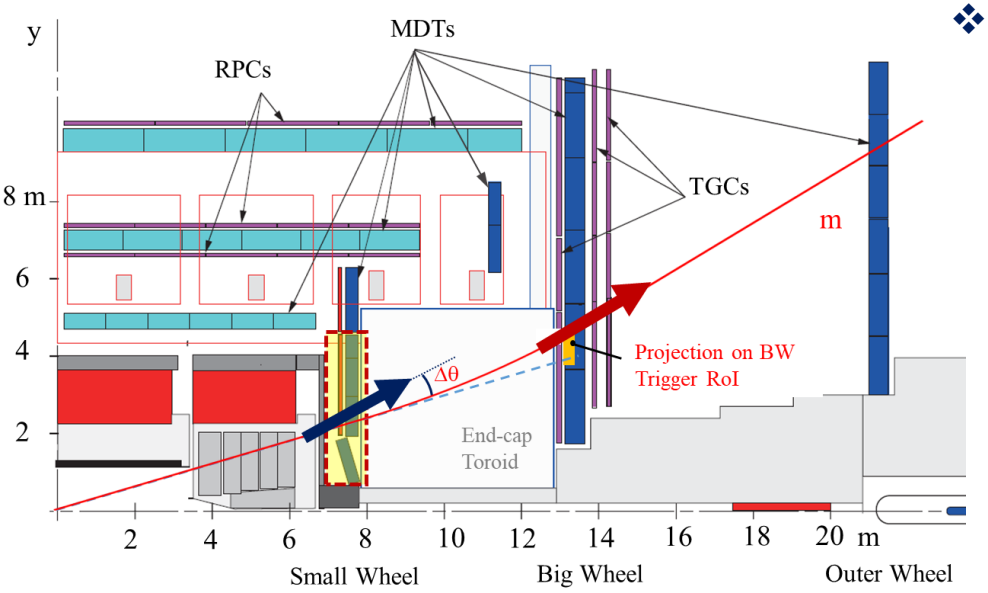
- The ATLAS New Small Wheel Upgrade replaces the innermost muon stations to:
  - Improve End-cap Level-1 trigger (up to $|\eta| = 2.4$) **Primary focus of the talk**
  - Maintain good muon tracking capability (P_T 10%@ 1TeV up to $|\eta| = 2.7$)

for LHC high luminosity runs with high pile-up backgrounds. Unable to handle with the present Muon Small Wheel!

Introduction – ATLAS Muon New Small Wheel Upgrade



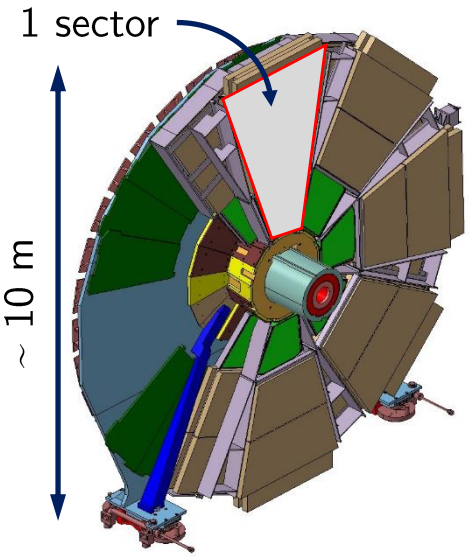


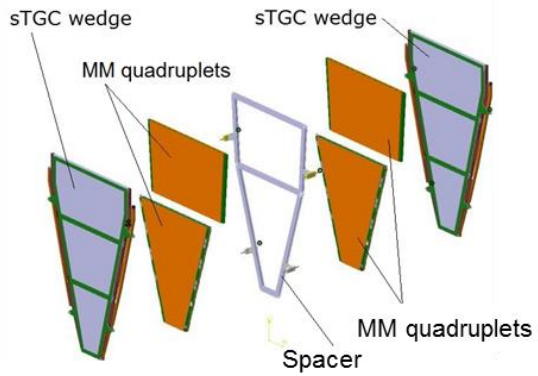


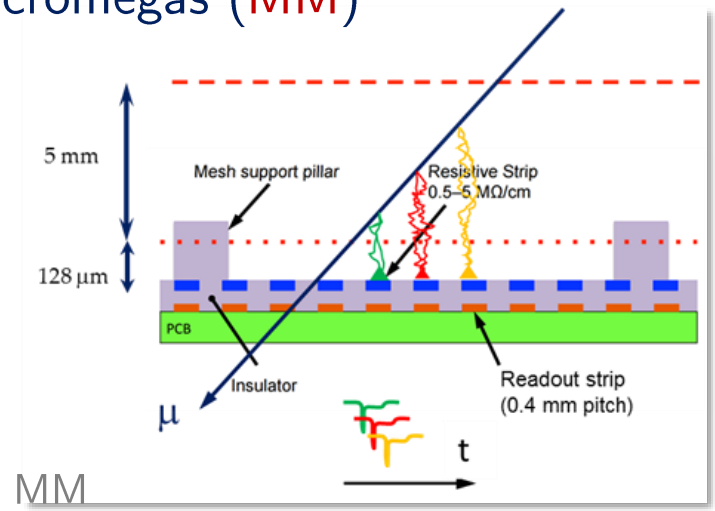
- Level-1 Muon Trigger after Phase-I upgrade: The NSW will provide on-line segment measurements to corroborate with Big Wheel segments. Eliminate non-IP originating backgrounds.
- NSW trigger requirement: 1 mrad online segment point accuracy, 1 μs (~500 ns for fiber) latency, 95% tracking efficiency

Introduction – ATLAS Muon New Small Wheel Upgrade

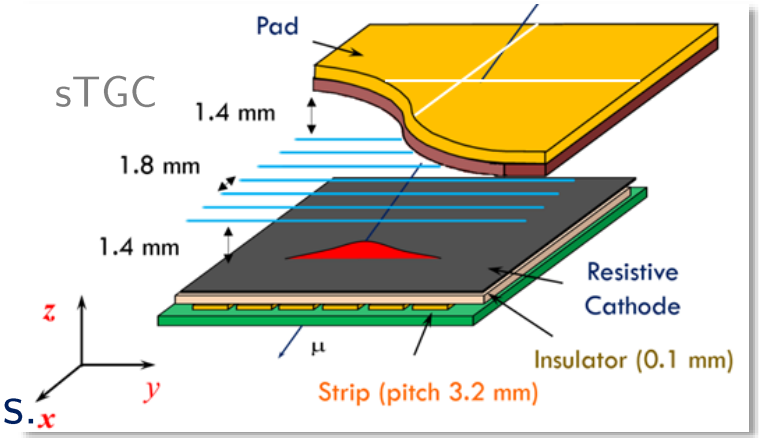
- NSW Detector Technologies:
  - Micromesh Gaseous Structure Detector, Micromegas (MM)
  - Small-strip Thin Gap Chamber (sTGC)







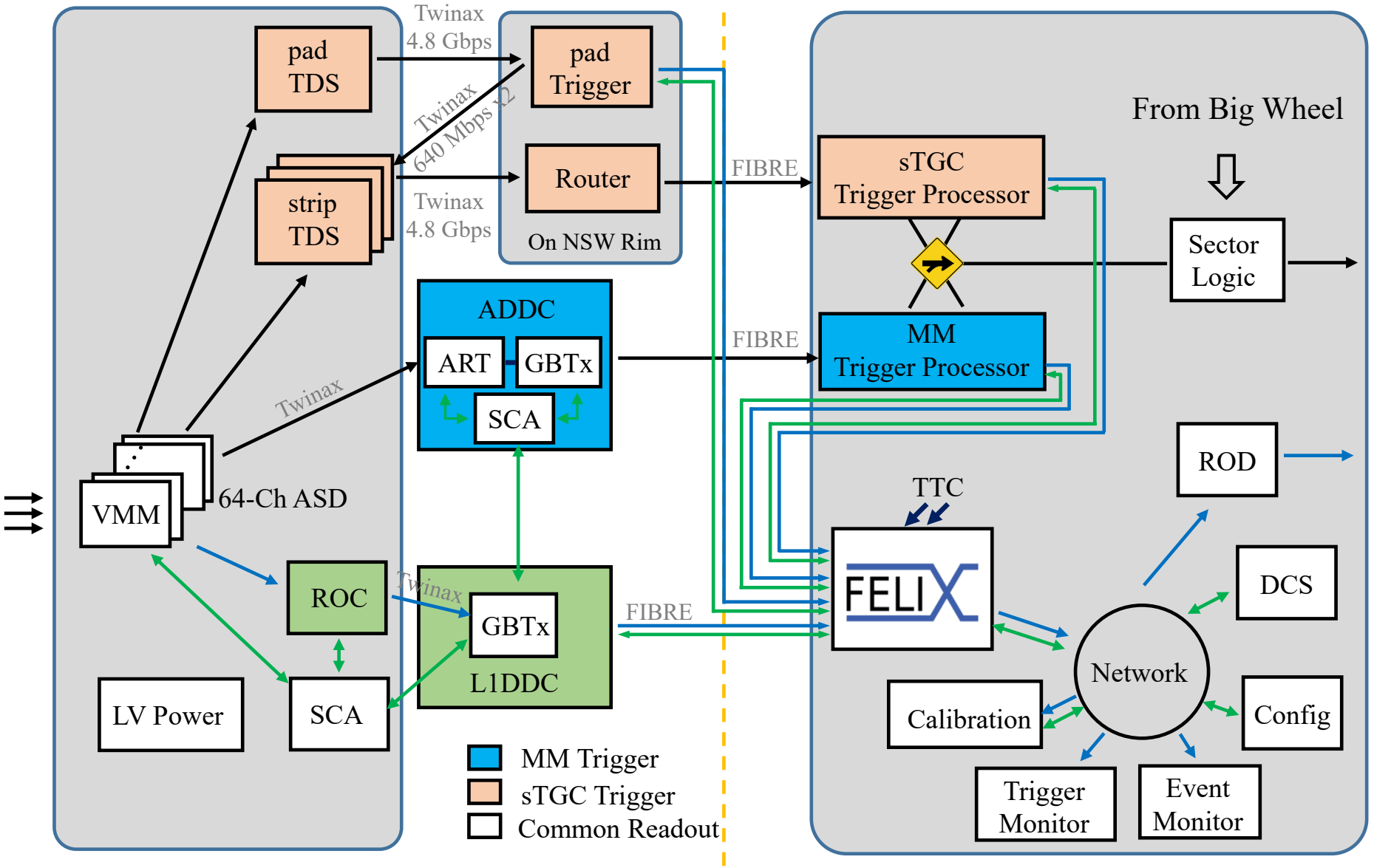
Readout channels:
- MM: ~ 2.1 M
- sTGC: 280k (strip) + 46k (pads) + 28k (wires)



- Both detector technologies to be used for trigger and tracking. Independency data paths.

⇨ Ensure redundancy over next ~20 yrs with very limited access!

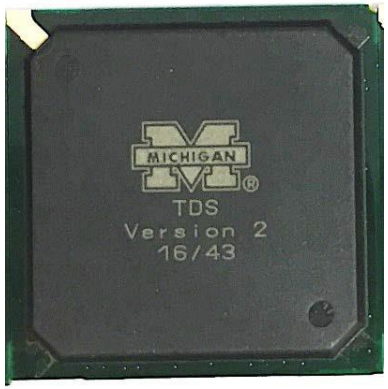
NSW Trigger and Readout Complex

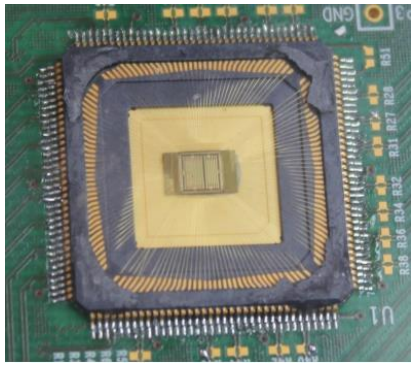


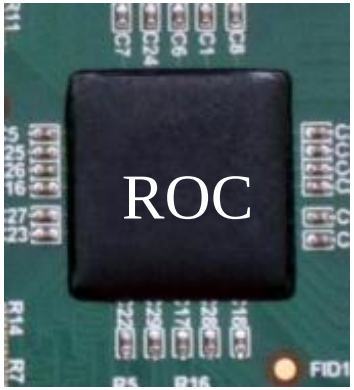
NSW ASICs

- Four ASICs will be developed for the NSW Trigger and Readout Chain
  - VMM: Front-end amplifier, shaper and discrimination chip with digital readout and L0* matching capabilities

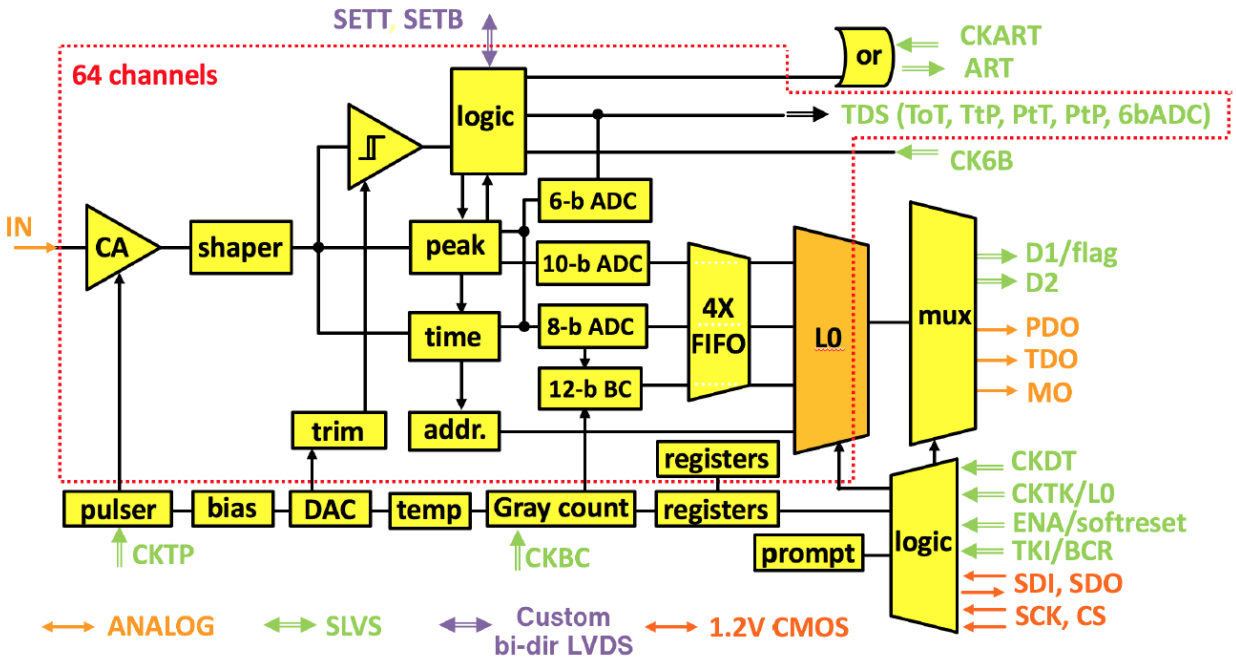
    (*ATLAS TDAQ introduces two level hardware based trigger for HL-LHC runs. L0 provides lowest level trigger up to 1 MHz)
  - TDS (Trigger Data Serializer): pre-L1 trigger, prepares trigger data for sTGC
  - ART (Address in Real Time): prepares trigger data for Micromegas
  - ROC (Readout Controller): distribute TTC to other ASICs, aggregate readout data

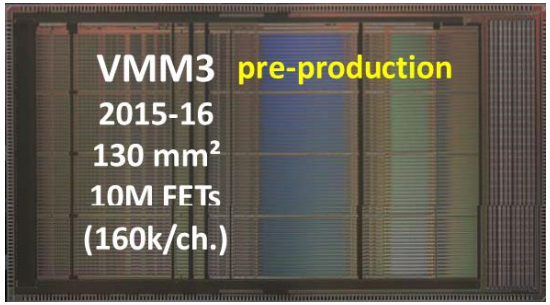






NSW ASICs: VMM



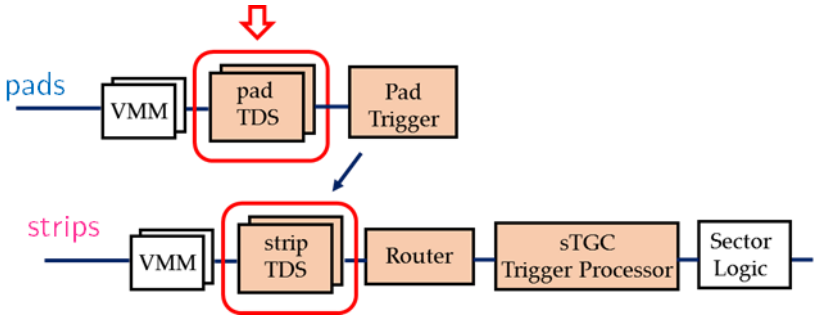


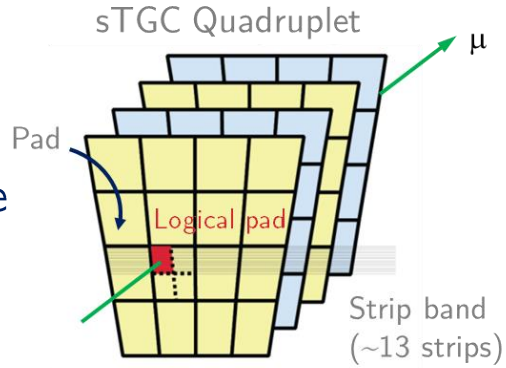
- Lower-power amplifier followed by 3rd shaper with complex conjugate poles in Delayed Dissipative Feedback. Selectable gain and peaking time.
- Three lower-power ADCs per channel for charge and time measurements: both trigger (6-bit charge and timing pulses) and readout (10bit charge)outputs
- Readout: buffer up to 64 events, L0 matching

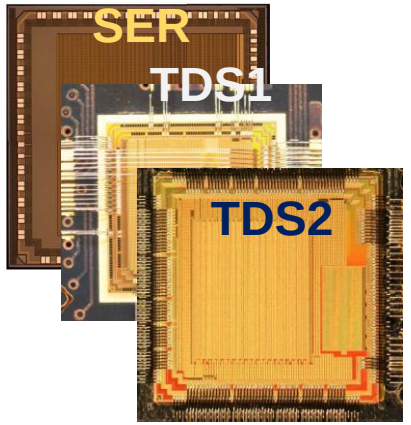
Channels	64
Polarity	Positive/negative
Zin	50-75 Ohm
Gain	0.5-16 mV/fC
Peaking time	25-200 ns
Shaper	Unipolar bipolar
Shaper order	3rd cc
TAC	60-650 ns
Time resolution	<1 ns
Power	10mW/channel

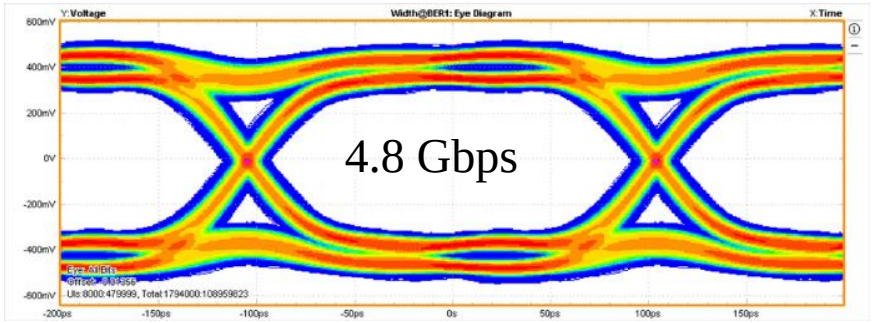
NSW ASICs: TDS for sTGC Triggering

- Impossible to send out all charge data from 300k sTGC strips for triggering.
- TDS ASIC preselect a band of strips under a pad "ROI" for Level-1 triggering
- Main specifications:
  - Two modes: strip/pad
  - 128 channels w/ individual programmable delay (pad-mode only)
  - Output data rate: 4.8 Gbps. Trigger data for every bunch crossing.
  - Radiation tolerant (logic TMR protected)
- Three prototypes fabricated and packaged. Production of 3000 chips to be launched soon.



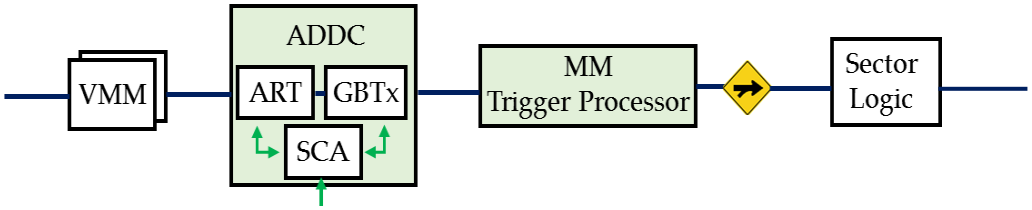


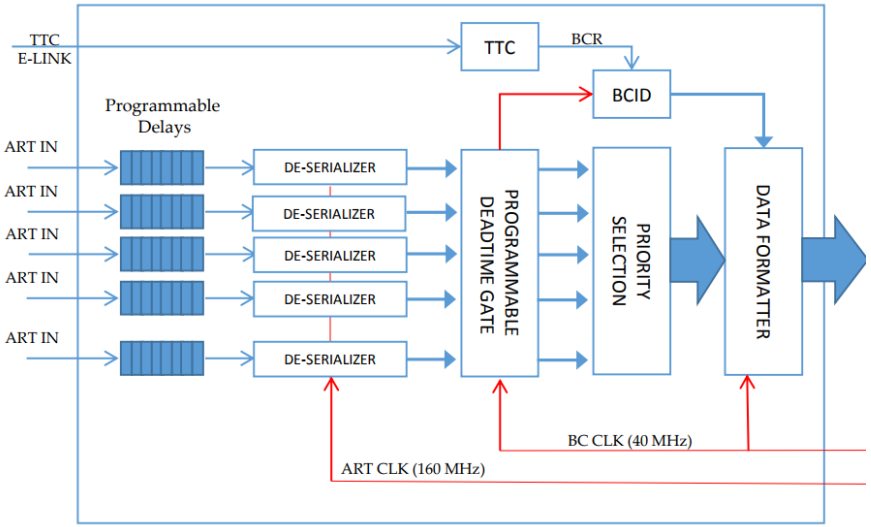




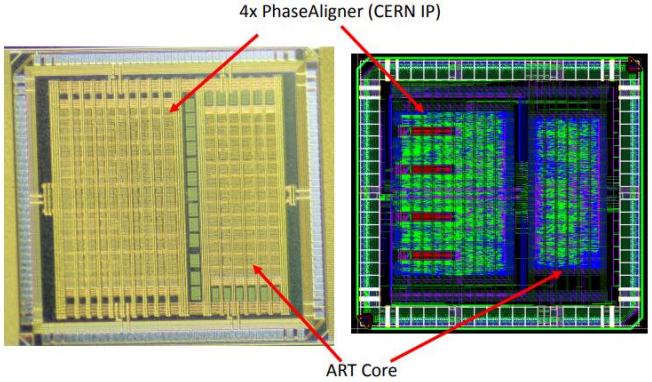
NSW ASICs: ART for Micromegas Triggering

- Micromegas utilizes fine strip pitch (0.4 mm) for precision triggering.
- The VMM ASIC provides the address of first threshold-crossing strip in an event
- The ART ASIC aggregates addresses from 32 VMMs and choses up to 8 hits to transmit
- Main Specifications:
  - Programmable delay
  - TTC/BCID counting
  - Priority-based hit selection and data formatting
- Two prototypes fabricated. Packaged chip testing on trigger board ongoing.

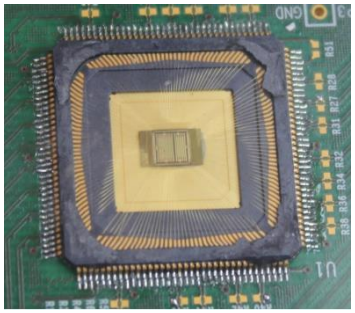




ART2 Silicon Die

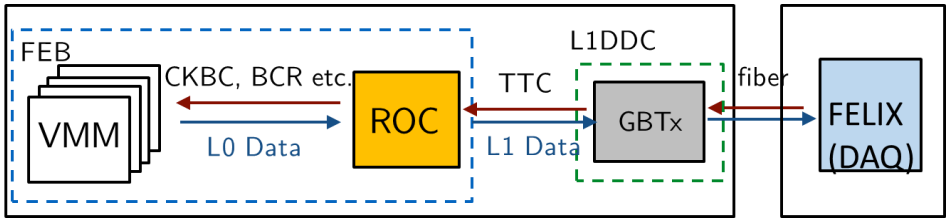


ART2 Test Packaging

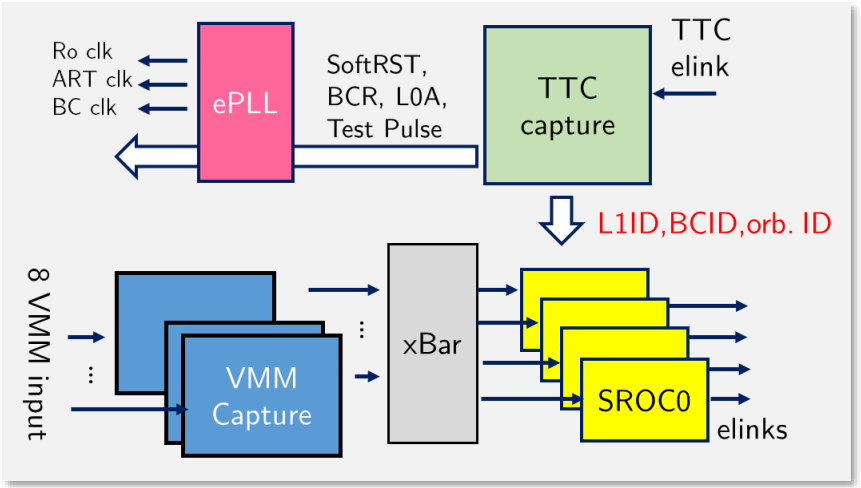


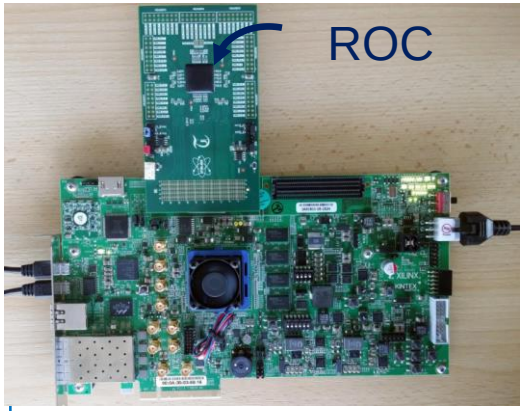
NSW ASICs: ROC

- The Readout Controller ASIC is responsible for providing "services" (Trigger, Timing, Control) to companion ASICs and aggregates Level-1 data from VMMs.



- Main specifications:
  - Distribute LHC 40 MHz clock, L0 accept, soft reset signals to VMM, TDS, ART ASICs
  - Decode serialized L0 data from up to 8 VMMs at up in 640 Mbps data rate
  - Data buffering and L1 trigger matching
  - Programable crossbar to balance output data links. Up to 8 elinks (up to 320 Mbps) for shifting data out.



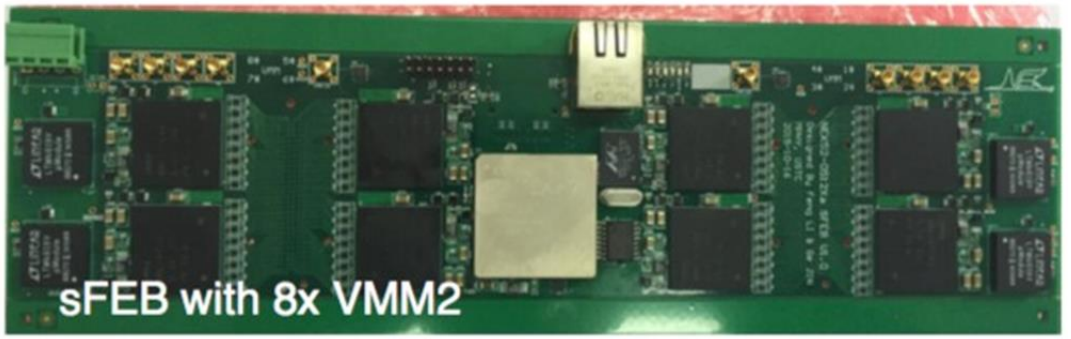


- Prototype fabricated and packaged. Systematic testing ongoing.

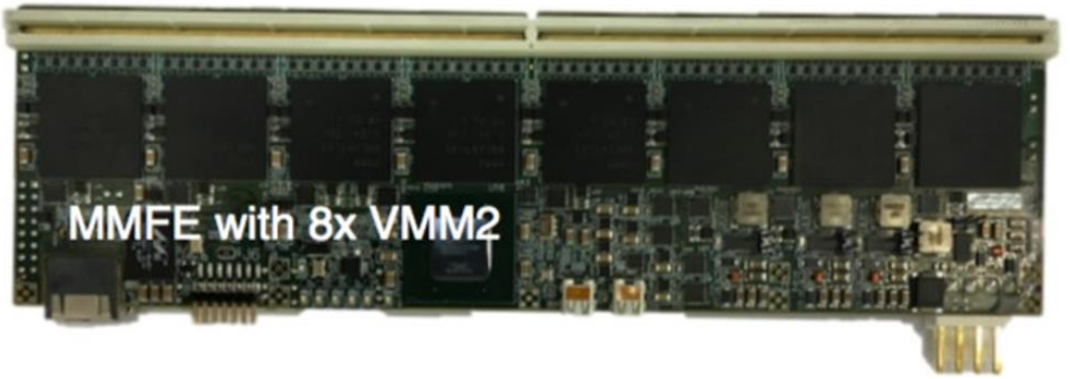
NSW On Detector Front-end Boards

- Front-end board will be populated with VMM, TDS, ROC ASICs plus two CERN-developed ASICs (GBT-SCA for slow control, DC-DC convertor named as "FEAST")

- Two types of FEBs (namely pFEB, sFEB) for sTGC to readout wires, pads and strips. One unique type for Micromegas

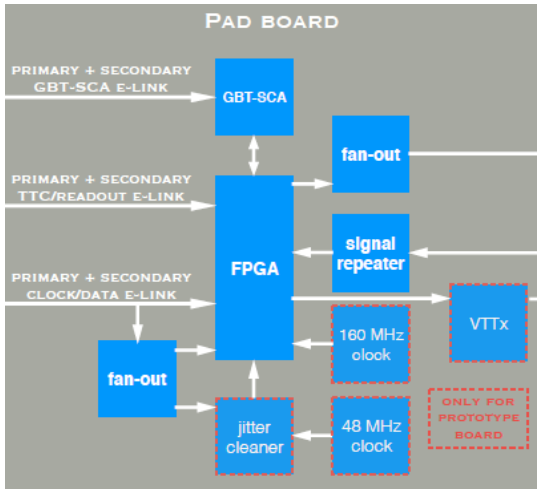


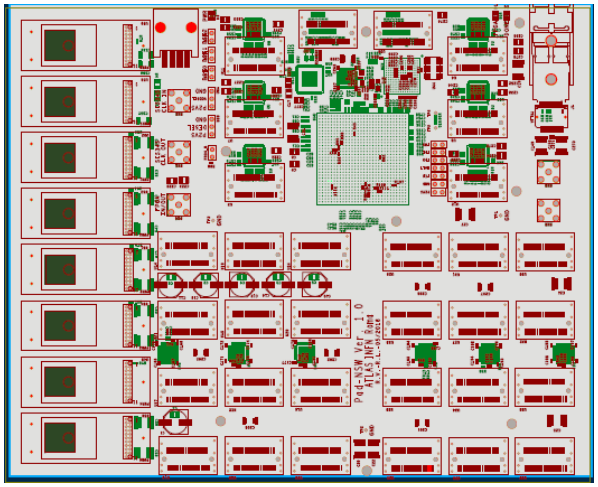
- More than 5000 boards on NSW. Challenging: Large number of readout channels with mixed (analog and fast digital) signals. Very complex layout and routing!



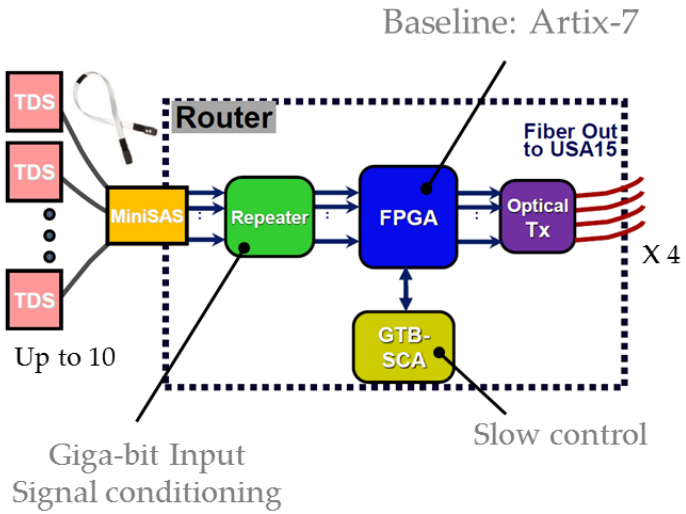
NSW On Detector Trigger Boards

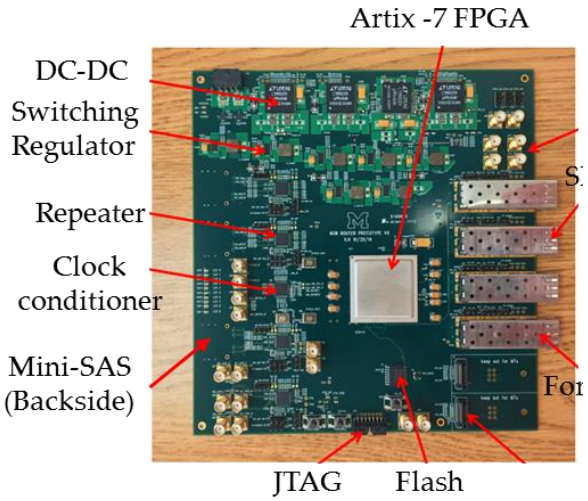
- **sTGC Pad Trigger Board**: perform 2 ¾ pad coincidences; send "ROI" together with BCID to strip-TDS for reading charge from active strips





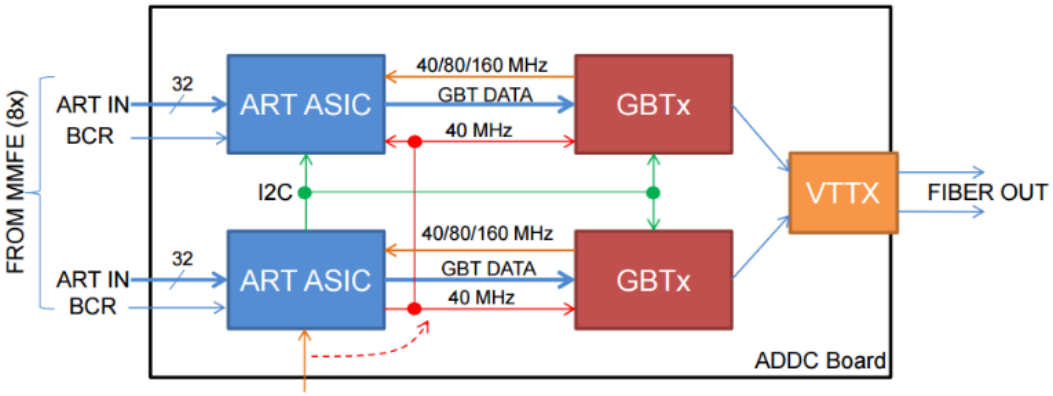
- **sTGC Router Board**: Collect data packets from active TDSs and transmit data to trigger processor via four optical links. One board per detector layer per sector (256 total)

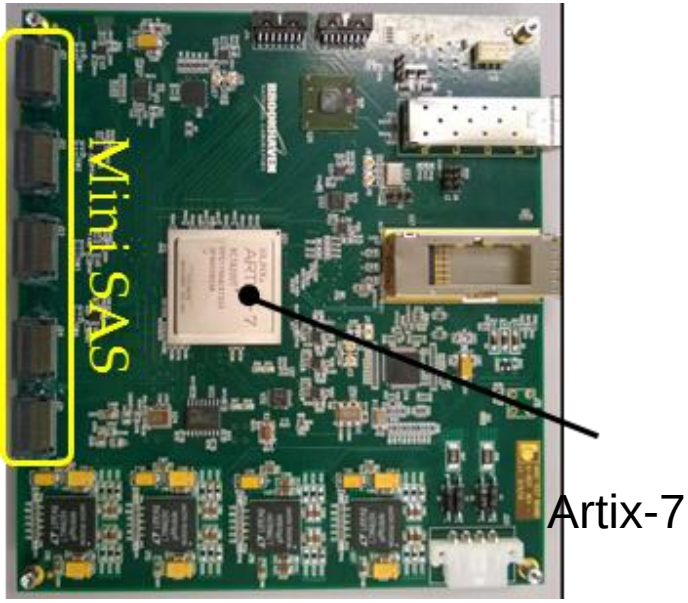




NSW On Detector Trigger Boards (Cont'd)

- **Micromegas ADDC Board**: Host two ART ASICs and transmit data via GBTx and VTTx (CERN rad. Hard. optical module)

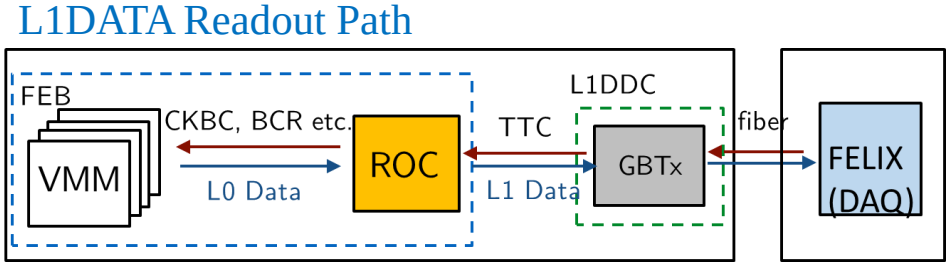


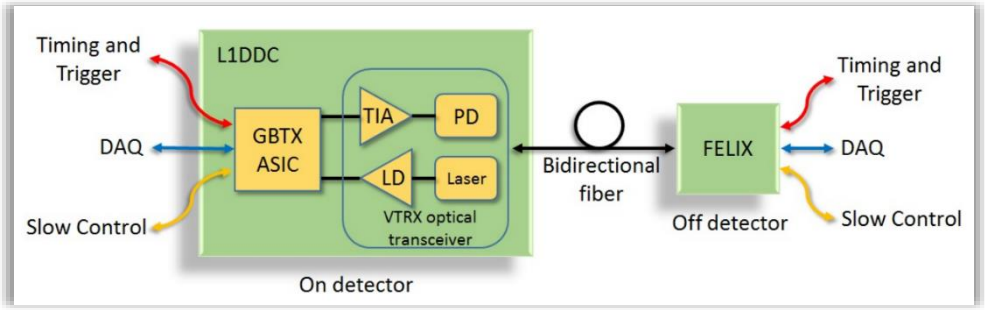


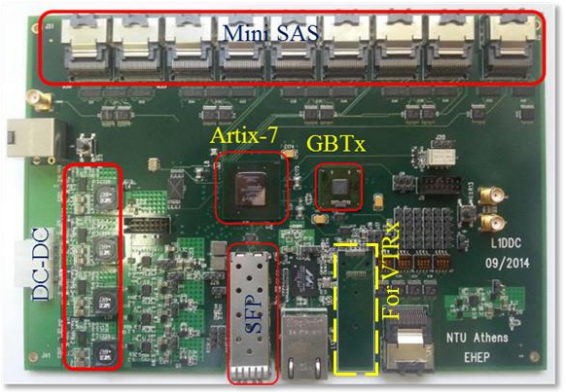
- **Status:** prototypes built for all boards. Production version to be launched at the end of the year

L1 Data Driver Card (L1DDC)

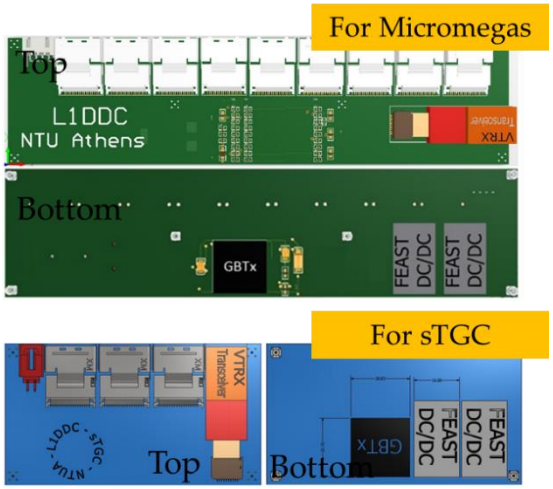
- L1DDC: Aggregates L1 readout data from FEBs and drive them to FELIX via fibers; Also used for config. & monitoring and TTC distribution





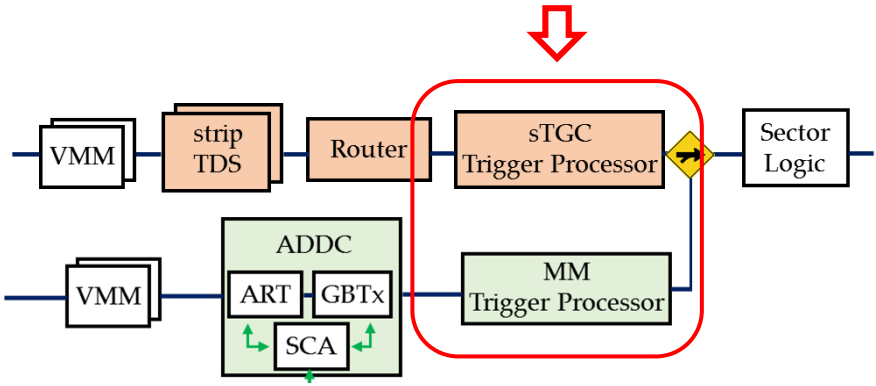


- CERN GBTx on board: rad. Hard bidirectional elinks w. programable speed on detector end. Output is 4.8 Gbps serialized link.
- Several types of boards developed: sTGC, Micromegas, plus RIM L1DDCs (for communicate with FEBs, sTGC Router and Pad Trigger Boards)

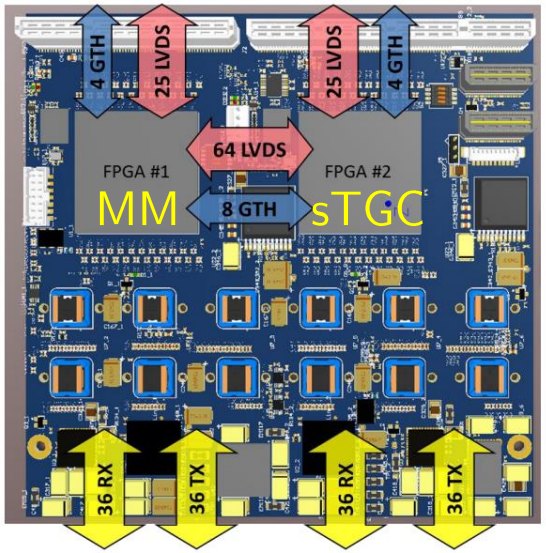


Trigger Processor Hardware Platform

- MM & sTGC trigger processor to be implemented on FPGA-based ATCA Mezzanine Cards
- Baseline: adopt ATCA Mezzanine card developed for Scalable Readout System* (SRS) platform
- 1 Mezzanine card for 1 NSW sector: 2 FPGAs, one for MM/sTGC trigger processor
- Mezzanine card main specification:
  - 32 input fibers (MM/sTGC)
  - 14 output fibers @ 6.4 Gbps+
  - Fast low latency link between MM and sTGC processors for lateral communication
- 1 ATCA carrier card hosts 2 Mezzanine cards (NSW sectors)



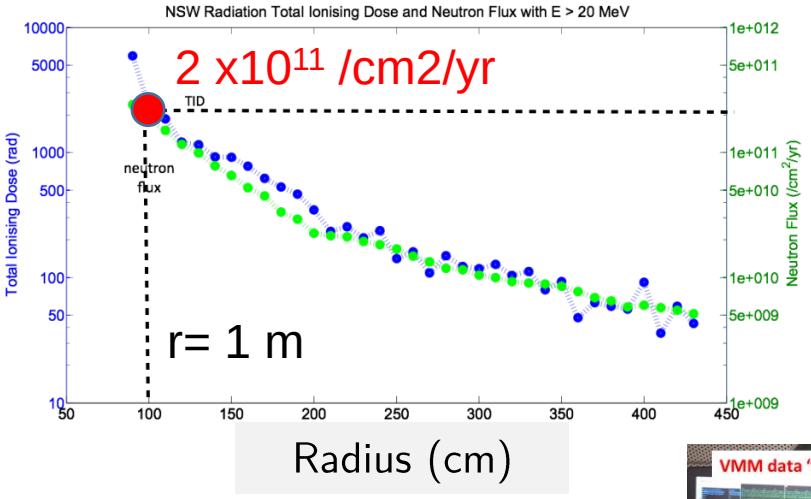
ATCA Mezzanine Card on SRS Platform



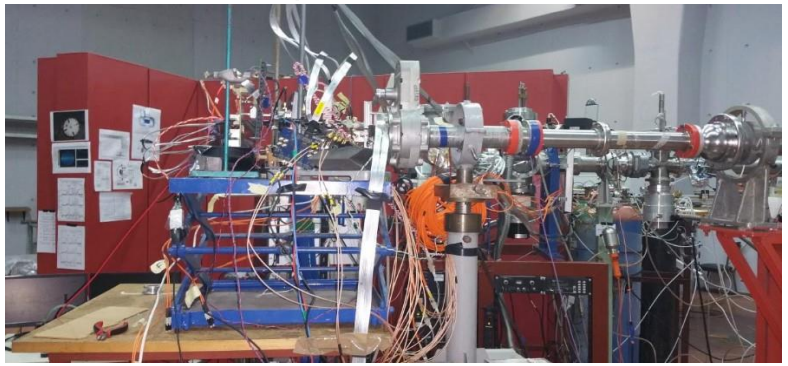
*S. Martoiu, et al., JINST 8.03 (2013): C03015.

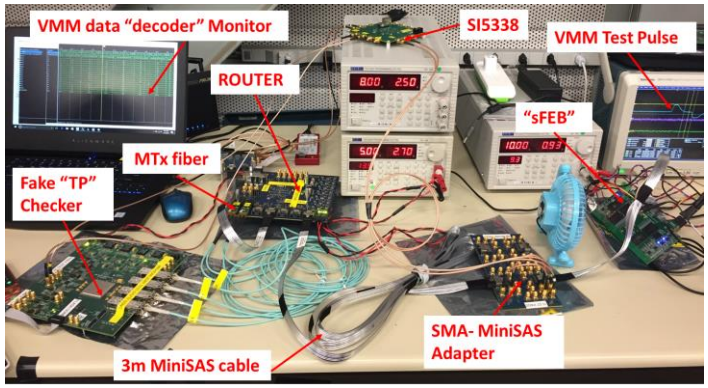
Electronics in Radiation Environment & Integration Efforts

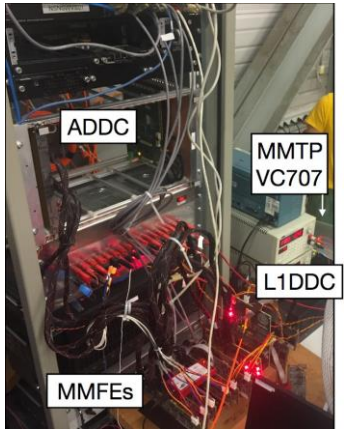
- Several campaigns to test TID, SEE of NSW ASICs, Electronics Boards under radiation environment.
- Most recent test at Demokritos: no configuration error, data link corruption for ROC, VMM, ADDC, L1DDC and Router with integration neutron flux equivalent to 1 year dose @ Innermost region NSW with $L=1x10^{34}$ $cm^{-2}s^{-1}$



Demokritos 20-24 MeV neutron beam







- Integration efforts: regular Integration weeks organized to put various parts together. Demonstration of data links in trigger and readout chain.

Conclusions and Outlook

- The New Small Wheel Upgrade is essential for ATLAS to improve the Level-1 trigger in order to maintain crucial physics program in high luminosity environment.
- A complex trigger and readout electronics system has been designed to achieve precise on-line muon segment measurements in the forward region of the Muon Spectrometer to discriminate against high-rate backgrounds.
- Significant efforts have been made in the design and verification of various radiation tolerant ASICs and electronic boards.
- Radiation tests and integration efforts are ongoing to qualify and realize the full trigger and readout chain. Progressing rapidly towards the full production of all parts at the end the year!

Thank you for your attention!